

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
15 August 2002 (15.08.2002)

PCT

(10) International Publication Number
WO 02/063543 A2

(51) International Patent Classification⁷: **G06K 7/10**

SMITH, George, S., II [US/US]; 3849 Oran Delphi Road, Manlius, NY 13104 (US).

(21) International Application Number: PCT/US02/01469

(22) International Filing Date: 18 January 2002 (18.01.2002)

(74) Agent: **BLASIAK, George, S.**; Wall Marjama & Bilinski LLP, Suite 400, 101 South Salina Street, Syracuse, NY 13202 (US).

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/766,806 22 January 2001 (22.01.2001) US
09/766,922 22 January 2001 (22.01.2001) US

(81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZM, ZW.

(71) Applicant (*for all designated States except US*): **HAND HELD PRODUCTS, INC.** [US/US]; 4619 Jordan Road, Skaneateles Falls, NY 13153 (US).

(72) Inventors; and

(75) Inventors/Applicants (*for US only*): **BARBER, Charles, P.** [US/US]; 5004 Lakeview Drive, Fayetteville, NY 13066 (US). **GARDINER, Robert, C.** [US/US]; 7274 Dabney Lane, Fayetteville, NY 13066 (US). **GERST, Carl, W., III** [US/US]; 119 Newbury Street, Apartment 4, Boston, MA 02116 (US). **HUSSEY, Robert, M.** [US/US]; 7274 Dabney Lane, Fayetteville, NY 13066 (US). **PANKOW, Matthew, W.** [US/US]; 18 Daniluk Drive, Camillus, NY 13031 (US).

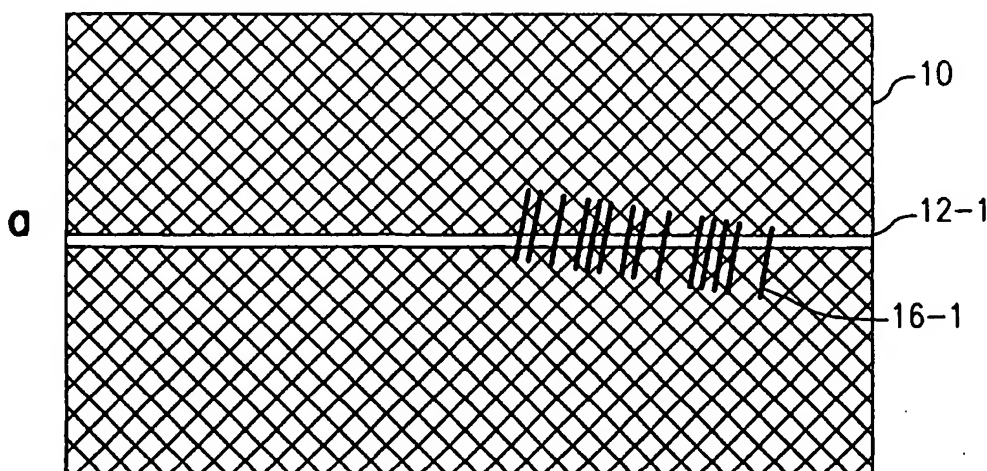
(84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— without international search report and to be republished upon receipt of that report

[Continued on next page]

(54) Title: OPTICAL READER HAVING PARTIAL FRAME OPERATING MODE



(57) Abstract: The invention is an optical reader having a 2D image sensor that is configured to operate in a partial frame capture mode. In a partial frame operating mode, the reader clocks out and captures at least one partial frame of image data having image data corresponding to less than all of the pixels of an image sensor pixel array. In one embodiment, the reader operating in a partial frame operating mode captures image data corresponding to a linear pattern of pixels of the image sensor, reads the image data, attempts to decode for a decodable 1D symbol which may be represented in the image data, and captures a full frame of image data if the image data reading reveals a 2D symbol is likely to be present in a full field of view of the 2D image sensor.



WO 02/063543 A2



For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

OPTICAL READER HAVING PARTIAL FRAME OPERATING MODE**Cross Reference to Related Applications:**

This PCT application claims the priority of U.S.

- 5 Application Serial No. 09/766,806, filed January 22, 2001,
entitled "Optical Reader Having Partial Frame Operating Mode,"
and U.S. Application Serial No. 09/766,922, filed January 22,
2001, entitled "Optical Reader Having Reduced Parameter
Determination Delay."

10

Field of the Invention

The invention relates to optical readers in general and
in particular to a method for operating an optical reader
having a 2D image sensor.

Background of the Prior Art

Optical readers having 2D image sensors commonly are used
to read both 1D and 2D symbols. Some optical readers having a
2D image sensor read a 1D symbol by capturing a 2D image
representation, or "frame" of image data corresponding to a
target area which comprises a 1D symbol, and launching a scan
line or lines in order to attempt to decode for 1D symbols
which may be represented in the area. Other optical readers
having 2D image sensors read 1D symbols by capturing a 2D
image representation of an area containing the 1D symbol,
preliminarily analyzing the image data represented in the area
to determine that the image data comprises a representation of
a 1D symbol, and then launching a scan line in an attempt to
decode for the 1D symbol determined to be present. In either
case, a full frame 2D image representation is captured in
order to decode for a 1D symbol.

Capturing a 2D image representation requires a substantial amount of time, especially in applications wherein one or more "test" frames of image data must be captured prior to capture of a frame that is subjected to processing. That is, prior to commencing comprehensive image data processing, which may include e.g. searching for symbol or character representations, decoding and character recognition processing, presently available optical readers clock out and capture in a memory location at least one exposure test frame of image data, read pixel data from the memory-stored exposure test frame to determine an exposure parameter value that is based on actual illumination conditions, then utilize the exposure parameter value in the exposure of a frame of image data that is clocked out, and then subjected to searching, decoding, and/or character recognition processing. The frame of image data exposed utilizing the exposure parameter based on actual illumination conditions is not available for reading until after it is clocked out. Presently available optical readers therefore exhibit an appreciable inherent exposure parameter determination delay. Readers having higher resolution imagers have slower frame clock out rates and therefore longer exposure parameter determination delays.

Furthermore, assuming a constant processing speed, the time required for an optical reader to capture a 2D image representation increases with the resolution of the image sensor which is incorporated in the reader. Currently available CMOS mega pixel image sensors have low frame clock out rates of about 15 frames per second (FPS).

A user's satisfaction with an optical reader often varies directly with the decoding speed of the optical reader. Given that higher resolution, including mega pixel readers, are

expected to grow in popularity, the frame capture time will become an increasingly important factor for consideration in performance of an optical reader.

Summary of the Invention

The invention is a method for configuring an optical reader having a 2D image sensor so the reader captures and processes image data at higher speeds.

According to the invention, a control circuit of an optical reader equipped with a 2D image sensor is configured to operate in a partial frame operating mode. In a partial frame operating mode, the control circuit clocks out and captures less than a full frame of image data and processes that image data. The control circuit may process the image data of the partial frame, for example, by reading the image data from memory and outputting the image data to an output location such as a display device or a processor system in communication with the reader, by reading and attempting to decode decodable symbols which may be recorded in the partial frame, or by reading and performing optical character recognition on characters represented in the partial frame of image data.

In one embodiment, the partial frame operating mode is employed to clock out and capture image data corresponding to at least one linear pattern sufficient so that a 1D symbol in the field of view of the image sensor may be decoded without clocking out and capturing an entire frame of image data. The partial frame of image data that is clocked out from the image sensor during the partial frame capture operating mode may be, for example, a row of symbols at or near the center of the image sensor or a limited number of lines of image data

corresponding to pixel locations of the image sensor, possibly at varying angular orientations. The control circuit may be configured so that if the control circuit cannot decode a 1D symbol during the course of operating in the partial frame capture mode, or detects that a 2D symbol is represented in the captured image data, the control circuit switches operation to a full frame capture mode.

In another embodiment, the partial frame operating mode is employed to clock out and capture pixel values corresponding to a grouping of pixels at or near a center of an image sensor other than a linear pattern of pixels. This embodiment may be advantageously employed in cases where decodable symbols are expected to be concentrated proximate a center of an image sensor's field of view. A control circuit may be configured so that if the control circuit cannot decode a symbol represented in the partial frame, or determines that a symbol is represented partially or entirely outside the image data of the partial frame, the control circuit automatically switches operation to a full frame image capture mode.

In further aspect of the invention, in one embodiment a partial frame mode of operation is executed to effect a reduction in a parameter determination delay. According to the invention in a parameter delay reduction-embodiment, an image sensor is adapted to clock out image data from an image sensor according to two modes of operation, a partial frame operating mode as has been described herein (which may also be referred to as a "low resolution" clock out mode of operation) which is executed during parameter determination and a full-frame operating or "normal resolution" clock out mode of operation.

In a low resolution mode, in one embodiment, as explained herein, some pixels of the reader's image sensor pixel array are clocked out at a normal clock out speed sufficient to develop electrical signals that accurately represent the intensity of light incident on the pixel array, while other pixels of the array are either not clocked out or are clocked out at a higher clock out rate which is insufficient to allow development of electrical signals that accurately represent the intensity of light at the respective pixels but which nevertheless, result in an increase in the overall frame clock out rate of the frame of image data. In a normal resolution mode of operation the image sensor is caused to clock out electrical signals corresponding to each pixel of the array at a constant "normal mode" speed which is a speed sufficient to ensure that the electrical signal corresponding to each pixel accurately represents the intensity of light incident on the pixel.

An optical reader according to the invention may operate an image sensor in a partial frame low resolution mode of operation in order to clock out and capture a parameter-determining frame of image data at high speed, may read pixel data from the parameter determination frame to determine an operation parameter based on actual illumination conditions, then utilize the operation parameter in operating an image sensor according to a normal resolution or "full frame" mode in the clocking out of a succeeding frame of image data that is captured and subjected to comprehensive image data processing which may include image data searching, decoding, and/or recognition processing. Clocking out some of the pixels of an array at high speed during execution of the partial frame or low resolution mode significantly decreases

the reader's parameter determination delay.

These parameters determined by reading pixel values from a partial or low resolution parameter determination frame of image data according to the invention may include an exposure time parameter, an amplification parameter for controlling amplification of an electrical signal prior to its analog to digital conversion, an illumination level parameter (intensity or period of illumination), a dark or light level adjustment parameter and an analog-to-digital converter reference voltage parameter for adjusting the high and/or low reference voltages of the reader's analog to digital converter.

These and other details, advantages and benefits of the present invention will become apparent from the detailed description of the preferred embodiment hereinbelow.

Brief Description of the Drawings

For a fuller understanding of the nature and objects of the present invention reference should be made to the following detailed description of the invention which is to be read in conjunction with the associated drawings wherein:

Figs. 1a-1e illustrate various image data patterns that may be captured by an optical reader operating in a partial frame capture mode according to the invention;

Fig. 2a is a block diagram of an optical reader of a type in which the invention may be incorporated;

Figs. 2b-2h show various types of optical reader housings in which the invention may be incorporated;

Fig. 3a is a process flow diagram illustrating frame clocking operations in an optical reader having an image sensor including a one-frame buffer;

Fig. 3b is a time line illustrating frame clock out

operations in a prior art optical reader;

Fig. 3c is a time line illustrating a frame clock out of operations in an optical reader operated according to the invention;

Figs. 4a and 4b are further image maps illustrating possible low resolution frames of image data clock out during a partial or low resolution frame clock out mode of the invention.

Detailed Description of the Invention

Referring to Figs. 1a-1g the invention is an optical reader equipped with a 2D image sensor that is configured to operate in a partial frame capture mode. In a partial frame clock out mode, a control circuit of an optical reader clocks out (or "reads") electrical signals corresponding to less than all of the 2D image sensor's pixels, and captures image data corresponding to the pixel locations into memory.

Partial frames of image data which may be clocked out and captured by an optical reader control circuit during a partial frame capture mode are illustrated in Figs. 1a-1g in which valid zones 12 represent frame image data corresponding to image sensor pixel positions that are clocked out and invalid zones 14 represent potential image data positions corresponding to pixel positions that are not clocked out.

Border 10 defines the full field of view of an optical reader in the case the reader is operated in a full frame captured mode while symbols 16-1, 16-2, 16-3, 16-4, 16-5, 16-6 and 16-7 are symbols entirely within the full field of view of an optical reader defined by border 10 but are only partially within certain valid zones shown. Valid zones 12-1, 12-3, 12-7, 12-8, 12-9, 12-10, and 12-13 are valid zones of image data

that partially contain representations of a decodable symbol while valid zones 12-11 and 12-12 are valid zones of image data captured during a partial frame capture mode which contain representations of an entire decodable symbol.

In the examples illustrated with reference to Figs. 1a-1e an optical reader operating in a partial frame clock out mode clocks out electrical signals corresponding to linear patterns of pixels. It is useful to cause a reader to clock out electrical signals corresponding to linear patterns as shown in Figs. 1a-1d when a reader will be used to decode mainly 1D linear bar code symbols.

In the examples illustrated with reference to Figs. 1f and 1g an optical reader operating in a partial frame clock out mode clocks out electrical signals corresponding to non-linear groupings of pixels. It is useful to cause a reader to clock out electrical signals corresponding to pixel groupings as shown in Figs. 1f and 1g when a reader will be used to decode symbols which are expected to be within a certain position in an image sensor's field of view.

A reader may be configured so that the reader automatically switches out of partial frame capture mode on the sensing of a certain condition. For example a reader according to the invention may be made to switch out of partial frame capture operating mode and into a full frame capture mode on the sensing that a 2D symbol is partially represented in the partial frame of image data, or on the condition that processing of the partial frame of image data fails to result in image data being decoded.

An optical reading system in which the invention may be employed is described with reference to the block diagram of Fig. 2a.

Optical reader 110 includes an illumination assembly 120 for illuminating a target object T, such as a 1D or 2D bar code symbol, and an imaging assembly 130 for receiving an image of object T and generating an electrical output signal indicative of the data optically encoded therein.

Illumination assembly 120 may, for example, include an illumination source assembly 122, together with an illuminating optics assembly 124, such as one or more lenses, diffusers, wedges, reflectors or a combination of such elements, for directing light from light source 122 in the direction of a target object T. Illumination assembly 120 may comprise, for example, laser or light emitting diodes (LEDs) such as white LEDs or red LEDs. Illumination assembly 120 may include target illumination and optics for projecting an aiming pattern 127 on target T. Illumination assembly 120 may be eliminated if ambient light levels are certain to be high enough to allow high quality images of object T to be taken. Imaging assembly 130 may include an image sensor 132, such as a 1D or 2D CCD, CMOS, NMOS, PMOS, CID OR CMD solid state image sensor, together with an imaging optics assembly 134 for receiving and focusing an image of object T onto image sensor 132. The array-based imaging assembly shown in Fig. 2a may be replaced by a laser array based imaging assembly comprising multiple laser sources, a scanning mechanism, emit and receive optics, at least one photodetector and accompanying signal processing circuitry.

The partial frame clock out mode is readily implemented utilizing an image sensor which can be commanded to clock out partial frames of image data or which is configured with pixels that can be individually addressed. Using CMOS fabrication techniques, image sensors are readily made so that

electrical signals corresponding to certain pixels of a sensor can be selectively clocked out without clocking out electrical signals corresponding to remaining pixels of the sensor. CMOS image sensors are available from such manufacturers as Symagery, Pixel Cam, Omni Vision, Sharp, National Semiconductor, Toshiba, Hewlett-Packard and Mitsubishi. A partial frame clock out mode can also be carried out by selectively activating a frame discharge signal during the course of clocking out a frame of image data from a CCD image sensor, as is explained herein.

Optical reader 110 of Fig. 2a also includes programmable control circuit 140 which preferably comprises an integrated circuit microprocessor 142 and an application specific integrated circuit (ASIC 144). The function of ASIC 144 could also be provided by a field programmable gate array (FPGA). Processor 142 and ASIC 144 are both programmable control devices which are able to receive, output and process data in accordance with a stored program stored in memory unit 145 which may comprise such memory elements as a read/write random access memory or RAM 146 and an erasable read only memory or EROM 147. RAM 146 typically includes at least one volatile memory device but may include one or more long term non-volatile memory devices. Processor 142 and ASIC 144 are also both connected to a common bus 148 through which program data and working data, including address data, may be received and transmitted in either direction to any circuitry that is also connected thereto. Processor 142 and ASIC 144 differ from one another, however, in how they are made and how they are used.

More particularly, processor 142 is preferably a general purpose, off-the-shelf VLSI integrated circuit microprocessor which has overall control of the circuitry of Fig. 2a, but

which devotes most of its time to decoding image data stored in RAM 146 in accordance with program data stored in EROM 147. Processor 144, on the other hand, is preferably a special purpose VLSI integrated circuit, such as a programmable logic or gate array, which is programmed to devote its time to functions other than decoding image data, and thereby relieve processor 142 from the burden of performing these functions.

The actual division of labor between processors 142 and 144 will naturally depend on the type of off-the-shelf microprocessors that are available, the type of image sensor which is used, the rate at which image data is output by imaging assembly 130, etc. There is nothing in principle, however, that requires that any particular division of labor be made between processors 142 and 144, or even that such a division be made at all. This is because special purpose processor 144 may be eliminated entirely if general purpose processor 142 is fast enough and powerful enough to perform all of the functions contemplated by the present invention. It will, therefore, be understood that neither the number of processors used, nor the division of labor there between, is of any fundamental significance for purposes of the present invention.

With processor architectures of the type shown in Fig. 2a, a typical division of labor between processors 142 and 144 will be as follows. Processor 142 is preferably devoted primarily to such tasks as decoding image data, once such data has been stored in RAM 146, recognizing characters represented in stored image data according to an optical character recognition (OCR) scheme, handling menuing options and reprogramming functions, processing commands and data received from control/data input unit 139 which may comprise such

elements as trigger 174 and keyboard 178 and providing overall system level coordination.

Processor 144 is preferably devoted primarily to controlling the image acquisition process, the A/D conversion process and the storage of image data, including the ability to access memories 146 and 147 via a DMA channel. Processor 144 may also perform many timing and communication operations. Processor 144 may, for example, control the illumination of LEDs 122, the timing of image sensor 132 and an analog-to-digital (A/D) converter 136, the transmission and reception of data to and from a processor external to reader 110, through an RS-232, a network such as an ethernet, a serial bus such as USB, a wireless communication link (or other) compatible I/O interface 137. Processor 144 may also control the outputting of user perceptible data via an output device 138, such as a beeper, a good read LED and/or a display monitor which may be provided by a liquid crystal display such as display 182. Control of output, display and I/O functions may also be shared between processors 142 and 144, as suggested by bus driver I/O and output/display devices 137' and 138' or may be duplicated, as suggested by microprocessor serial I/O ports 142A and 142B and I/O and display devices 137' and 138'. As explained earlier, the specifics of this division of labor is of no significance to the present invention.

Some or all of the above optical and electronic components may be incorporated in an imaging module as are described in commonly assigned Application Serial No. 09/411,936, incorporated herein by reference.

Figs. 2b-2g show examples of types of housings in which the present invention may be incorporated. Figs. 2b-2g show 1D/2D optical readers 110-1, 110-2 and 110-3. Housing 112 of

each of the optical readers 110-1 through 110-3 is adapted to be graspable by a human hand and has incorporated therein at least one trigger switch 174 for activating image capture and decoding and/or image capture and character recognition operations. Readers 110-1 and 110-2 include hard-wired communication links 179 for communication with external devices such as other data collection devices or a host processor, while reader 110-3 includes an antenna 180 for providing wireless communication device or a host processor.

In addition to the above elements, readers 110-2 and 110-3 each include a display 182 for displaying information to a user and a keyboard 178 for enabling a user to input commands and data into the reader. Control circuit 140 may cause a graphical user interface (GUI) to be displayed on display 182. A pointer on the GUI may be moved by an actuator or actuators protruding from housing 112.

Any one of the readers described with reference to Figs. 2b-2g may be mounted in a stationary position as is illustrated in Fig. 2h showing a generic optical reader 110 docked in a scan stand 190. Scan stand 190 adapts portable optical reader 110 for presentation mode scanning. In a presentation mode, reader 110 is held in a stationary position and an indicia bearing article is moved across the field of view of reader 110.

As will become clear from the ensuing description, the invention need not be incorporated in a portable optical reader. The invention may also be incorporated, for example, in association with a control circuit for controlling a non-portable fixed mount imaging assembly that captures image data representing image information formed on articles transported by an assembly line, or manually transported across a checkout

counter at a retail point-of-sale location. Further, in portable embodiments of the invention, the reader need not be hand held. The reader may part or wholly hand worn, finger worn, waist worn or head worn for example.

Referring again to particular aspects of the invention, control circuit 140 in the example of Fig. 1a executes a partial frame capture mode in order to clock out and capture pixel data illustrated by valid zone 12-1. Reading the pixel values of valid zone 12-1 is effective to decode 1D symbol 16-1 in the reader's full field of view. Given that clocking out and capturing image data of valid zone 12-1 consumes less time than clocking out and capturing a full frame of image data, it is seen that execution of a partial frame capture mode decreases the decode time of the reader. In prior art 2D optical readers, electrical signals corresponding to full frame 10 are clocked out in order to decode a single 1D symbol 16-1. The pixels of valid zone 12-1 may comprise a single row of pixels (a scan line) or a plurality of rows.

In the example of Fig. 1b, of control circuit 40 executes a partial frame capture mode in order to capture data defining valid zones 12-2, 12-3 and 12-4 of a full frame of image data corresponding to a full field of view of a 2D image sensor. Valid zones 12-2, 12-3 and 12-4 are line patterns of image data at various angular orientations. Reading of pixels of line valid zones arranged at various angular orientations is effective to decode a 1D symbol which may be located at an oblique angle in a field of view. It is seen that reading of pixels of line valid zone 12-3 will result in the successful decoding of 1D bar code symbol 16-2. Zones 12-2, 12-3 and 12-4 may be one or more pixels

wide.

In the example of Fig. 1c, control circuit 40 executes a partial frame capture mode in order to clock out and capture image data defining valid zones 12-5 and 12-9. Valid zones 12-5 to 12-9 form a plurality of horizontal parallel lines. The pattern of valid zones shown in Fig. 1c clocked out and captured in a partial frame capture mode is effective for decoding substantially horizontally oriented 1D symbols which are at an unknown height in a full field of view. It is seen that the reading of image data of valid zone 12-8 will not result in the decoding of symbol 16-3 because symbol 16-3 is not a 1D symbol. Nevertheless, because valid zone 12-8 intersects symbol bullseye 16b, reading of a image data of valid zone 12-8 may be effective to determine that a 2D symbol is likely present in the full field of view of image sensor 132. In one aspect of the invention, reader 110 may be configured to switch out of a partial frame capture mode and into a full frame capture mode when reading of image data captured in the partial frame capture mode reveals that a 2D symbol is likely to be represented in the image data corresponding to the image sensor's full field of view.

The states of operation of reader 110 operating in accordance with the invention are normally selected by actuating appropriate buttons of keyboard 178, or control of a GUI, or by the reading of menuing symbols, as are explained in commonly assigned Patent No. 5,929,418 incorporated herein by reference.

It should be apparent that several operating states of the invention are possible. In a first operating state, reader 10 is made to operate only in a partial frame capture mode until the time the first operating state is deactivated.

In a second operating state, as is alluded to in the example of Fig. 1c, the reader operates in a partial frame capture mode until the time that reading of image data captured in the partial frame capture mode reveals that a 2D symbol is likely to be included in the full frame field of view of image sensor 132. When reading of the partial frame of image data reveals that a 2D symbol is likely to be included in a full frame field of view, control circuit 40 captures at least one full frame of image data from sensor 132 and attempts to decode for the 2D symbol determined likely to be represented in the full frame of image data. A reader operating in the second operating state may also be made to switch to a full frame operating mode on the condition that a symbol is not successfully decoding during operation of the reader in the partial frame operating mode.

A third operating state of a reader operating in accordance with the invention is described with reference to Figs. 1d and 1e. Operating in accordance with a third operating state, a reader operates in a partial frame capture mode to clock out and capture image data of valid zone 12-10 which corresponds to a predetermined pattern and position in field of view 10. It is seen that reading of image data of zone 12-10 will not be effective to decode symbol 16-4 because symbol 16-4 is of a type of 2D symbol known as a stacked linear bar code. Control circuit 140 may nevertheless detect that symbol is a 2D symbol given that valid zone 12-10 intersects a finder pattern 16f of symbol 16-4.

Sensing that a 2D symbol is likely present in the field of view when reading the partial frame image data corresponding to valid zone 12-10, the reader operating in the third operating state then continues to operate in a partial frame mode to clock

out and capture image data that defines a second valid zone 12-11 of pixel positions as seen in Fig. 1e. The second valid zone 12-11 is not of a predetermined size and position, but rather is of an adaptive position whose position, and possibly size, orientation and shape depends on the result of the reading of the image data corresponding to the first valid zone 12-10. Specifically, the second valid zone 12-11 is normally at least of a size and position that is likely to encompass the symbol 16-4 detected to be present when reading of the image data of first valid zone 12-10. It is seen that the third operating state is likely to be operative to further reduce the clocking out and capture of irrelevant image data, and therefore is likely to further increase decoding speed. In the third operating state, additional adaptive position valid zones may be clocked out and captured if the reading of image data of first adaptive valid zone 12-11 does not result in a symbol being decoded.

In the example of Figs. 1f and 1g valid zones 12-12 and 12-13 correspond to nonlinear groupings of pixels. Capturing of the valid zone patterns 12-12 and 12-13 of Figs. 1f and 1g is particularly useful for decoding symbol image data in the case that a symbol is likely to be at a certain position in relation to an image sensor's full frame field of view such as in the center of an image sensor's field of view as shown in Fig. 1f.

In the example of Fig. 1f control circuit 140 can successfully decode symbol 16-6 because symbol 16-6 is located entirely within valid zone 12-12.

In the example of Fig. 1g, control circuit 140 cannot decode symbol 16-7 if operating in the first operating state since symbol 16-7 is a 2D symbol and is not entirely located within

valid zone 12-13. If operating in the second operating state, then a reader capturing image data within valid zone 12-13 may successfully decode symbol 16-7 by reading the image data of zone 12-13 to determine that a 2D symbol is present, switching operation to a full frame capture mode to capture a full frame 10 of image data, and processing the full frame of image data to decode symbol 16-7. A reader operating in the third operating state described herein above may decode symbol 16-7, in the example of Fig. 1g, by reading image data within valid zone 12-13, capturing image data within an adaptively defined valid zone (not shown) of sufficient size and position to encompass symbol 16-7, and then processing the image data within the adaptively defined valid zone to decode symbol 16-7.

A partial frame operating mode of the invention is useful for reducing a parameter determination delay as will now be described herein. When operated to generate valid pixel data, presently available optical reading devices clock out electrical signals corresponding to pixel positions of an image sensor at a uniform clock out rate such that the electrical signal corresponding to each pixel of the image sensor array accurately represents light incident on the pixel.

By contrast, an image sensor of the present invention as has been described herein is made to operate under two major frame capture modes, a partial or "low resolution" frame clock out mode and a "normal resolution" or full frame clock out mode. In one embodiment of a partial frame or "low resolution" mode of operation, an image sensor according to the invention is operated to clock out electrical signals corresponding to some pixels of an image sensor array at a high clock out rate and other pixels

of the image sensor at a normal clock out rate. Clocking out a portion of the electrical signals using a faster than normal clock out rate results in a reduction in the overall frame clock out time while clocking out a portion of the signals at a normal clock out rate enables the generation of pixel data sufficient to enable determination of parameter settings for use in subsequent frame captures. In a full frame or "normal resolution" mode of operation in one embodiment the image sensor is operated to clock out electrical signals corresponding to pixels of the array using a single uniform clock out speed as in prior art readers. The low resolution mode of operation may also be carried out by clocking out electrical signals corresponding to only a portion of a frame's pixels and not clocking out electrical signals corresponding to the remaining pixels.

A reader configured in accordance with the invention adapted to reduce a parameter determination delay clocks out and captures in a memory storage location at least one parameter determination frame of image data in a partial frame or "low resolution" frame capture mode, reads pixels of the parameter determination frame in establishing at least one operation parameter that is based on actual illumination conditions, utilizes the determined operation parameter in clocking out a subsequent frame of image data in a full frame or "normal resolution mode," then captures and subjects the frame of image data clocked out utilizing the operation parameter to image data searching, decoding, and/or recognition processing.

Referring to particular aspects of the invention, a partial or low resolution frame clock out mode of the invention is described in detail with reference to the pixel maps of Figs. 4a

and 4b. Control circuit 40 establishes a clock out rate for clocking out an electrical signal corresponding to a pixel of an image sensor 32 by appropriate state control of control signals in communication with image sensor 32. In the present invention, in one embodiment, image sensor 32 is selected to be of a type whose pixel clock out rate can be varied by way of control signals received from control circuit 40. In presently available optical readers, an image sensor's pixel clock out rate is not changed during the course of clocking out of a frame of image data.

In a partial frame or "low resolution" frame clock out mode of the invention, however, control circuit 40 in one embodiment of the invention causes image sensor 32, to clock out electrical signals corresponding to the pixels of the array at least two speeds during a single frame capture period. During a single frame clock out period, in a possible partial frame operating mode, control circuit 40 controls image sensor 32 so that some pixels are clocked out at normal clock out rate sufficient to develop electrical signals accurately representing the intensity of light at the respective pixel positions, while other pixels are either not clocked out or are clocked out at a clock out rate which may be insufficient to allow development of electrical signals that accurately represent the intensity of light at the respective pixels but which nevertheless results in a reduction of the overall frame clock out time of the frame of image data being clocked out.

Fig. 4a shows a schematic diagram of an exemplary image map frame that is clocked out according to the partial frame or low resolution frame clock out mode of the invention and then

captured into memory 45. The image map is divided into "zones" of valid data and invalid data. Valid zones 84 shown are rows of pixels that are clocked out at a normal clock out speed while invalid zones 86 shown are rows of pixel that are clocked out at a faster clock out speed, which is normally (but not necessarily) a speed insufficient to allow development of electrical signals accurately representing the intensity of light at a pixel. It is seen that the pattern of valid zones 84 in Fig. 4a is similar to the pattern of valid zones 12-5, 12-6, 12-7, 12-8 and 12-9 of Fig. 1c.

Fig. 4b shows another possible division of an image map into valid zones and invalid zones. This type of embodiment in which valid zones 84 comprise less than full pixel rows is conveniently realized by appropriate control of an image sensor manufactured using CMOS fabrication methods. Using CMOS fabrication methods, an image sensor can be merged with a microprocessor, an ASIC, or another timing device on a single die to the end that a preestablished clocking sequence in which a pixel clock out rate is changed multiple times during the course of clock out a frame of image data may be actuated in response to the activation of a single control signal in communication with image sensor 32.

Using CMOS fabrication techniques, image sensors can be readily made so that electrical signals corresponding to certain pixels of a sensor can be selectively clocked out without clocking out electrical signals corresponding to remaining pixels of the sensor to generate valid and invalid zones of image data within a single frame of image data as described herein. CMOS image sensors are available from such manufacturers as Symagery, Pixel Cam, Omni Vision, Sharp, Natural Semiconductor, Toshiba,

Hewlett-Packard and Mitsubishi.

The invention is also conveniently realized with use of an image sensor having an image sensor discharge function. Image sensors having a discharge function are typically adapted to receive a discharge clock out signal which when active results in all pixels of a frame being read out at a high clock out rate insufficient to allow development of electrical signals. In presently available readers having a directional function, a control circuit sets the discharge clocking signal to an active state while clocking out an initial "discharge period" frame of image data immediately after reception of a trigger actuation. This initial discharge process removes any residual charges built up on image sensor 32 prior to capturing a first frame including valid pixel data.

For producing an image map divided into valid and invalid zones using an image sensor having a discharge function, control circuit 40 may be made to intermittently change the state of a discharge clock out signal during a frame clock out period during which image sensor 32 is otherwise operated according to a normal resolution clock out or full frame operating mode.

An exemplary embodiment of the invention in which the invention is employed in a reader equipped with a SONY ICX084AL CCD image sensor (that includes a one frame analog buffer memory) and a SONY CXD2434TQ timing generator is described with reference to Figs. 3a, 3b and 3c. Fig. 3a shows a flow diagram, of an imaging system in which the image sensor includes a one frame buffer memory. For purposes of illustrating the advantages of the invention, Fig. 3b shows a time line illustrating the time required to clock out and capture a frame of image data useful

for searching and decoding in a prior art reader having a buffer memory not configured to operate in accordance with a low resolution frame clock out mode. Fig. 3c shows a time line illustrating the time required to clock out and capture a frame of image data useful for searching, decoding, and recognizing characters in a reader having a buffer memory configured to operate in a low resolution frame clock out mode according to the invention.

When a reader includes a one frame buffer memory, then the activation of an appropriate frame clock out signal by image sensor 32 causes electrical charges representative of light on pixels of an image sensor's pixel array 32a to be transferred to analog buffer memory 32b and causes electrical signals corresponding to pixel value storage locations of buffer 32b (representing light on the pixels during a previous timing period) to be clocked out to analog to digital converter 36 so that the frame of image data stored on buffer memory can be captured in memory 45, wherein the data may be read by control circuit 40.

Referring to time line 92 corresponding a prior art reader it can be seen that a substantial parameter determination delay is present without use of a low resolution frame capture mode according to the invention. At time T0, control circuit 40 activates a frame discharge control signal so that residual charges built up in the storage locations of buffer memory 32b are eliminated or "cleaned" during clock out period CPO.

At time T1, control circuit 40 activates a frame clocking signal to commence the clock out a first frame of pixel data according to a normal resolution frame clock out mode (the pixel

data clocked out during clock out period CP1 is normally invalid pixel data). During clock out period CP1, the charges built up on pixel array 32a during clock out period CP0 are transferred to buffer memory 32b and then clocked out to A/D converter 36. Also during clock out period CP1 pixel array 32a is exposed to light for a time determined by an exposure parameter value, e_0 , that was previously transmitted at time Te_0 prior to time $T1$. The exposure parameter e_0 is based on previous exposure values during a previous trigger actuation period or based on expected illumination conditions, but is not based on actual illumination conditions present.

At time $T2$, control circuit 40 activates a frame clock out signal to commence the clock out of a second frame of image data in accordance with a normal resolution frame clock out mode. During clock out period CP2, the charges built up on pixel array 32a during clock out period CP1 are transferred to buffer memory 32b and then clocked out to A/D converter 36. Also during clock out period CP2 pixel array 32 is exposed to light for a time determined by an exposure parameter value, e_1 , that was previously transmitted at time Te_1 prior to time $T2$. The exposure parameter e_1 , like exposure parameter e_0 , also cannot be based on actual illumination conditions since the most recent frame image data available for reading by circuit 40 prior to the transmittal of exposure parameter e_1 is the invalid frame data resulting from transmittal of frame discharge signal at time $T0$.

At time $T3$, control circuit 40 activates a frame clock out signal to commence the capture of a third frame of image data in accordance with a normal resolution frame clock out mode. During clock out period CP3, the charges built up on pixel array 32a

during clock out period CP2 are transferred to buffer memory 32b and then clocked out to A/D converter 36. Also during clock out period CP3, pixel array 32a is exposed to light for a time determined by an exposure parameter value, e_2 , that was previously transmitted at time Te_2 prior to time T3. Unlike the previous exposure values e_0 and e_1 , the exposure parameter value e_2 can be a value determined from actual illumination conditions since the frame of image data resulting from pixel array 32a being exposed to light during clock out period CP1, is available for reading by control circuit 40 prior to the time that the exposure parameter e_2 must be communicated to image sensor 32. However, because of the built in one frame delay resulting from the presence of buffer 32b, it is seen that a frame of image data clocked out while being exposed with the exposure parameter value e_2 , determined based on actual illumination conditions, will not be available for reading by control circuit unit after the expiration of clocking period CP4. Accordingly, it can be seen that the above reader exhibits a typical parameter determination delay of four normal resolution clock out periods, CP1+CP2+CP3+CP4 plus the frame discharge clock out parameter CP0. The normal resolution frame clock out rate of the above-referenced SONY image sensor is about 33.37 ms and the frame discharge rate is about 8.33 ms, resulting in a typical-case total parameter determination delay in the example described of 140ms (an earlier frame may be subjected to image data searching, decoding, and recognition if e_0 or e_1 yields an image of acceptable quality).

Advantages of operating image sensor 32 according to a partial frame operating or low resolution frame clock out mode of

operation are easily observable with reference to time line 94 corresponding to a reader having an image sensor operated in accordance with a low resolution frame clock out mode. In the example illustrated by time line 94 control circuit 40 operates image sensor as described in connection with Fig. 3b except that control circuit 40 operates image sensor 32 according to a low resolution frame clock out mode during clocking periods CP1, CP2, and CP3. Because electrical signals corresponding to only some of the pixels during these timing periods are clocked out at speeds sufficiently slow to read valid image data, the total frame clock out time association with these clocking periods is significantly shorter than that of a frame clocked out according to a normal resolution frame clock out mode. In an exemplary embodiment in which control circuit 40 alternately changes the state of a discharge clock out control signal (known as an EFS signal) in communication with a SONY ICX084AL CCD image sensor, to result in a zone division pattern having valid zones comprising four pixel rows clocked out at normal speed bounded by invalid rows having eighteen rows of pixels clock out at high speed, the low resolution frame clock out rate is 8.52 ms. The overall typical parameter determination delay is therefore reduced to $T_0+T_1+T_2+T_3+T_4=66.2$ ms as compared to the 140 ms delay in the prior art reader example described with reference to Fig. 3a.

In the example described in which image sensor 32 comprises a one frame buffer 32b, pixel array 32a is exposed to light for at least some time currently as electrical signals are clocked out from buffer 32b. In the control of presently available image sensors that do not have one frame buffers, frame clock out

periods normally follow frame exposure periods without overlapping the exposure periods.

A low resolution parameter determination frame of image data clocked out using a partial frame or low resolution clock out mode is useful for determining an exposure control parameter because exposure parameter values can be accurately determined by sampling only a small percentage of pixel values from a frame of image data. In fact, for improving the processing speed of an optical reader it is preferred to determine an exposure control value based on a sampling of a small percentage of pixel values from a frame of image data. The proper exposure parameter setting varies substantially linearly with illumination conditions, and therefore is readily determined based on a sampling of pixel values from a single frame of image data.

Additional reader operating parameters can be determined by reading pixel values from a frame of image data clocked out according to a partial frame or low resolution clock out mode of the invention. These additional parameters which may be determined from a low resolution parameter determining frame of image data include an amplification parameter for adjusting the gain of an amplifier prior to analog-to-digital conversion, an illumination level parameter for adjusting the current level delivered to, and therefore the radiance of light emitted from LEDs 22, an illumination time parameter for adjusting the on-time of LEDs 22, a light level parameter for adjusting a light level of a subsequently captured frame of image data, a dark level parameter for adjusting a dark level, of a subsequently captured frame of image data, and an analog-to digital converter reference parameter for adjusting a reference voltage of analog-to-digital

converter 36.

While the present invention has been explained with reference to the structure disclosed herein, it is not confined to the details set forth and this invention is intended to cover any modifications and changes as may come within the scope of the following claims:

In the Claims

1 1. A method of operating an optical reader having a 2D
2 image sensor array, said method comprising the steps of:

3 (a) controlling said image sensor array to generate a
4 plurality of electrical signals corresponding to pixels of
5 said image sensor array, wherein said plurality of generated
6 electrical signals accurately represent an intensity of light
7 incident on said pixels of said array for less than all of
8 said pixels of said array;

9 (b) capturing a partial frame of image data from said 2D
10 image sensor corresponding to said plurality of electrical
11 signals generated at step (a); and

12 (c) processing image data of said partial frame of image
13 data.

1 2. The method of claim 1, wherein said capturing step
2 includes the step of capturing image data corresponding to a
3 linear pattern of pixels.

1 3. The method of claim 1, wherein said capturing step
2 includes the step of capturing image data corresponding to a
3 plurality of angularly offset linear patterns of pixels.

1 4. The method of claim 1, wherein said capturing step
2 includes the step of capturing image data corresponding to a
3 plurality of vertically spaced apart horizontally oriented
4 linear patterns of pixels.

5 5. The method of claim 1, wherein said capturing step
6 includes the step of capturing image data corresponding to a

7 grouping of pixels about a center of said image sensor.

1 6. The method of claim 1, wherein said processing step
2 includes the step of reading said image data out of a memory
3 device.

1 7. The method the claim 1, wherein said processing step
2 includes the steps of reading said image data out of a memory
3 device and attempting to decode for a decodable symbol which
4 may be represented in said image data.

1 8. The method of claim 1, wherein said method further
2 includes the step of capturing a full frame of image data if
3 said processing step reveals that a 2D symbol is likely
4 partially represented in said partial frame of image data.

1 9. The method of claim 1, wherein said method further
2 includes the step of capturing an adaptively positioned
3 partial frame of image data if said processing step reveals
4 that a 2D symbol is likely partially represented in said
5 partial frame of image data.

1 10. The method of claim 1, wherein said processing step
2 includes the step of attempting to decode for a decodable
3 symbol represented in said image data, said method further
4 including the step of capturing a full frame of image data if
5 said processing step reveals that a 2D symbol is likely
6 partially represented in said partial frame of image data.

1 11. A method for operating an optical reader having a 2D
2 image sensor, said method comprising the steps of:

- 3 (a) in a partial frame operating mode, capturing a
4 partial frame of image data;
5 (b) attempting to decode a symbol representation of
6 said captured partial frame of image data; and
7 (c) switching operation of said reader to a full
8 frame capture mode if said reader fails to decode a symbol
9 representation in step (b).

1 12. The method of claim 11, wherein said capturing step
2 includes the step of capturing image data corresponding to a
3 linear pattern of pixels.

1 13. The method of claim 11, wherein said capturing step
2 includes the step of capturing image data corresponding to a
3 plurality of angularly offset linear patterns of pixels.

1 14. The method of claim 11, wherein said capturing step
2 includes the step of capturing image data corresponding to a
3 plurality of vertically spaced apart horizontally oriented
4 linear patterns of pixels.

1 15. The method of claim 11, wherein said capturing step
2 includes the step of capturing image data corresponding to a
3 grouping of pixels about a center of said image sensor.

1 16. A method for operating an optical reader having an
2 image sensor, said method comprising the steps of:
3 clocking out at least one frame of image data in a low
4 resolution frame clock out mode of operation;
5 reading pixel values from said at least one frame
6 clocked- out in said low resolution clock out mode to

7 determine an operating parameter of said reader; and
8 utilizing said operating parameter in operating said
9 reader.

1 17. The method of claim 16, wherein said low resolution
2 mode clock out step includes the step of clock out electrical
3 signals corresponding to some pixel values of said image
4 sensor at a higher than normal clock out rate so that an
5 overall frame clock out rate is increased.

1 18. The method of claim 16, wherein said low resolution
2 mode clock out step includes the steps of clocking out some
3 rows of said image sensor array at a normal clock out rate and
4 other rows of said image sensor at a higher than normal clock
5 out rate.

1 19. The method of claim 16, wherein said low resolution
2 clock out step includes the step of selectively clocking out
3 electrical signals corresponding to some pixels of said image
4 sensor and not clocking out electrical signals corresponding
5 to other pixels of said sensor.

1 20. The method of claim 16, wherein said image sensor
2 includes a discharge function actuated by activation of a
3 discharge control signals, wherein said low resolution mode
4 clock out step include the step of intermittently activating
5 said discharge control signal while clocking out a frame of
6 image data.

1 21. The method of claim 16, wherein said operating
2 parameter is an exposure parameter value.

1 22. The method of claim 16, wherein said operating
2 parameter is an illumination intensity value.

1 23. The method of claim 16, wherein said operating
2 parameter is an illumination on-time value.

1 24. The method of claims 16, wherein said operating
2 parameter is an amplifier gain parameter value.

3 25. The method of claim 16, wherein said operating
4 parameter is a dark level adjustment value.

1 26. The method of claim 16, wherein said operating
2 parameter is a light level adjustment value.

1 27. The method of claim 16, further comprising the step
2 of decoding a decodable symbol representation represented in a
3 frame of image data developed utilizing said operating
4 parameter.

1 28. The method of claim 16, wherein said frame clocked
2 out in said low resolution frame clock out mode is clocked out
3 to produce a low resolution parameter determination frame of
4 image data in which valid and invalid data zones are defined
5 by rows of said image sensor.

1 29. The method of claim 16, wherein said image sensor
2 includes a one frame buffer and wherein said low resolution
3 clock out step includes the step of clocking out three frames
4 of image data in a low resolution frame clock out mode.

1 30. A method for operating an optical reader having an
2 image sensor, said method comprising the steps of:
3 switching operation of said reader to a low resolution
4 mode of operation; and
5 in said low resolution mode, clocking out electrical
6 signals corresponding to some pixel values of said image
7 sensor at a higher than normal clock out rate so that an
8 overall frame clock out rate is increased.

1 31. The method of claim 30, wherein said clock out step
2 includes the steps of clock out some rows of said image sensor
3 array at a normal clock out rate and other rows of said image
4 sensor at a higher than normal clock out rate.

1 32. The method of claim 30, wherein said image sensor
2 includes a discharge function actuated by activation of a
3 discharge control signals, wherein said clock out step include
4 the step of intermittently activating said discharge control
5 signal while clock out a frame of image data.

1 33. A method for operating an optical reader having an
2 image sensor, said method comprising the steps of:
3 switching operation of said reader to a low resolution
4 mode of operation; and selecting in said low resolution mode,
5 clocking out electrical signals corresponding to some pixels
6 of said image sensor and not clocking out electrical signals
7 corresponding to other pixels of said image sensor.

1 34. An optical reader comprising:
2 an imaging assembly having an image sensor;
3 a controller, wherein said controller is adapted to clock

4 out at least one low resolution frame of image data, wherein
5 said controller is adapted to read pixel values from said at
6 least one low resolution frame of image data to determine an
7 operating parameter of said reader, and wherein said
8 controller is adapted to utilize said operating parameter in
9 operating said reader.

1 35. The reader of claim 34, wherein said controller
2 develops said low resolution frame of image data by clocking
3 out electrical signals of said frame at a higher than normal
4 rate.

1 36. The reader of claim 34, wherein said controller
2 develops said low resolution frame of image data by not
3 clocking out electrical signals corresponding to some pixels
4 of said frame.

1 37. The reader of claim 34, wherein said operating
2 parameter is an exposure parameter value.

1 38. The method of claim 34, wherein said operating
2 parameter is an illumination intensity value.

1 39. The method of claim 34, wherein said operating
2 parameter is an illumination on-time value.

1 40. The method of claims 34, wherein said operating
2 parameter is an amplifier gain parameter value.

1 41. The method of claim 34, wherein said operating
2 parameter is a dark level adjustment value.

1 42. The method of claim 34, wherein said operating
2 parameter is a light level adjustment value.

1 43. The reader of claim 34, wherein said controller is
2 further adapted to decode a decodable symbol representation
3 represented in a frame of image data developed utilizing said
4 operating parameter.

1 44. The reader of claim 34, wherein said imaging
2 assembly includes an illumination assembly.

1 45. The reader of claim 34, wherein said illumination
2 assembly includes white LEDs.

FIG. 1a

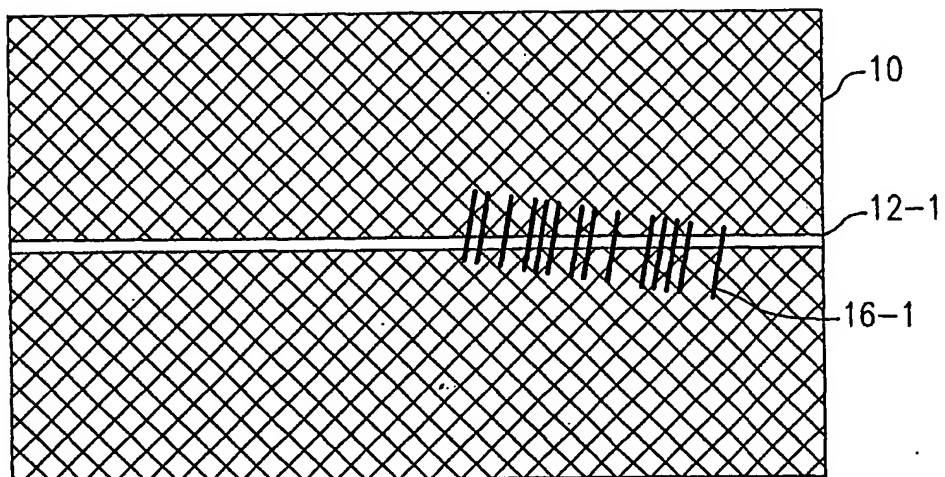


FIG. 1b

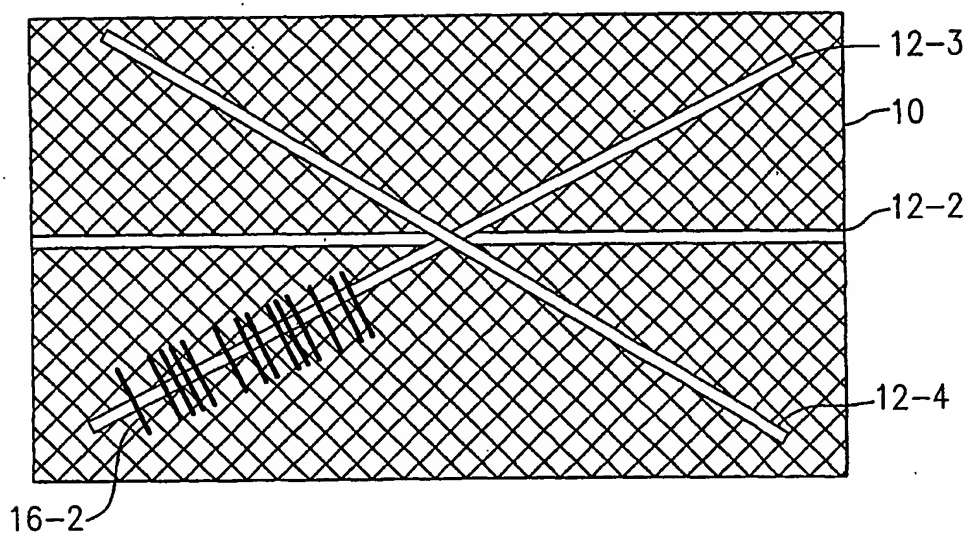
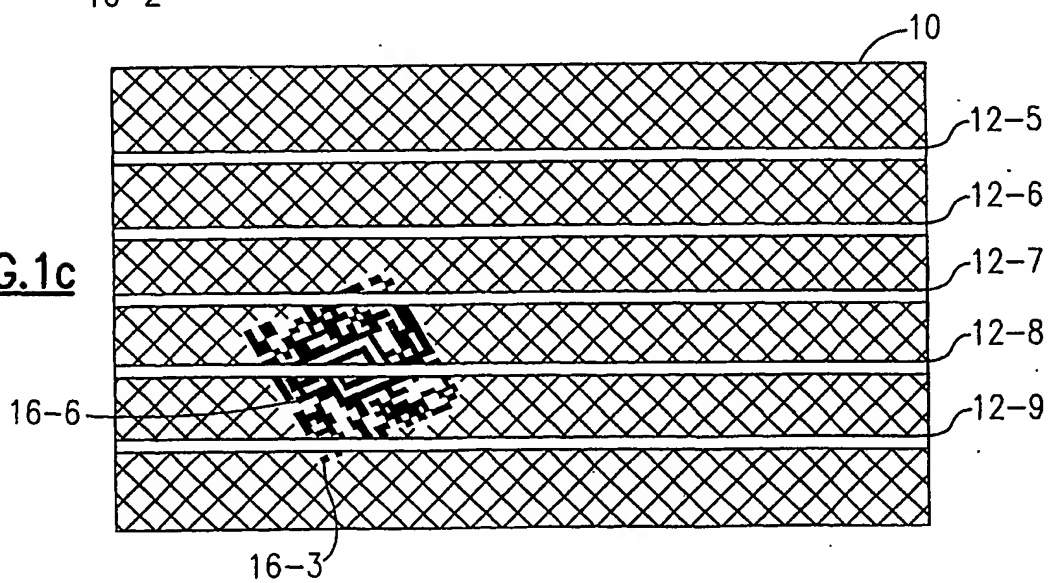


FIG. 1c



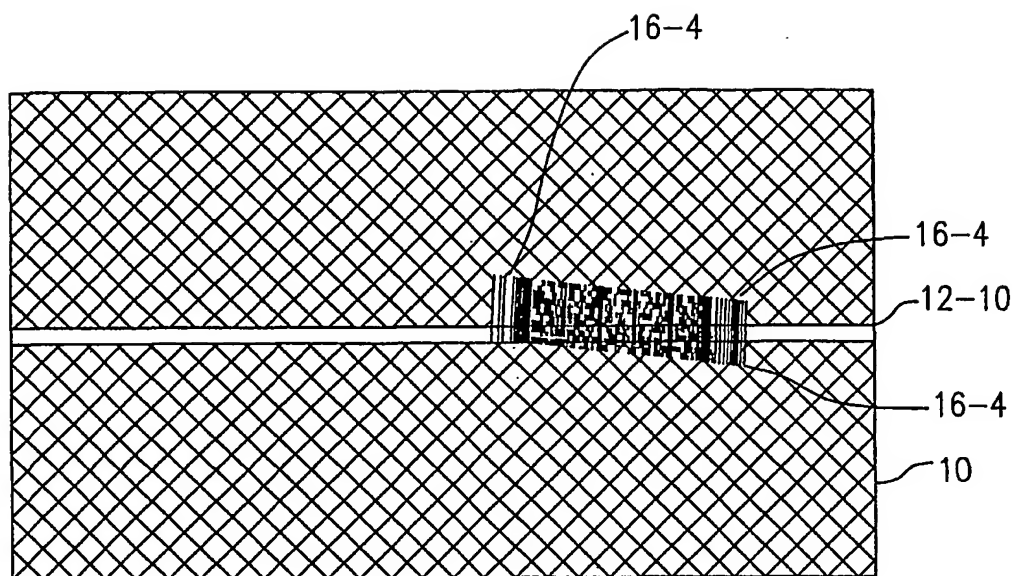


FIG. 1d

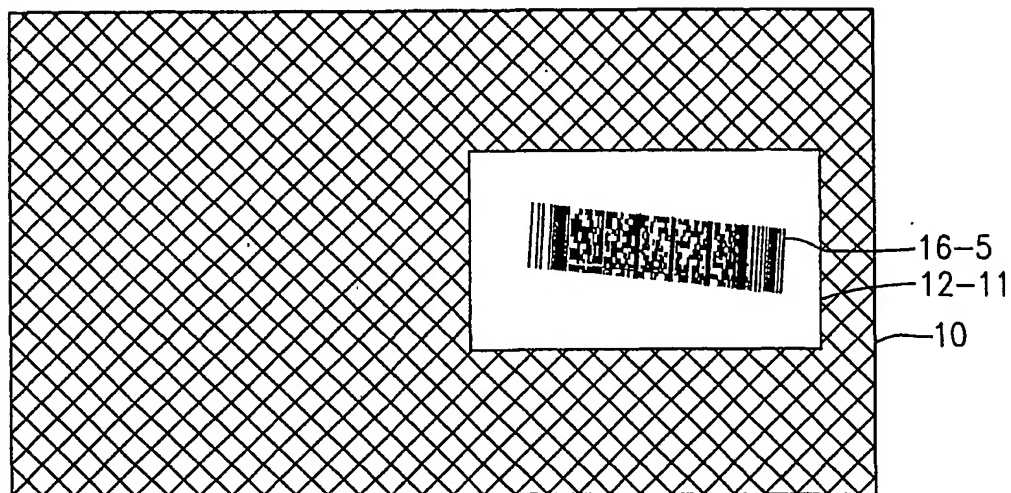


FIG. 1e

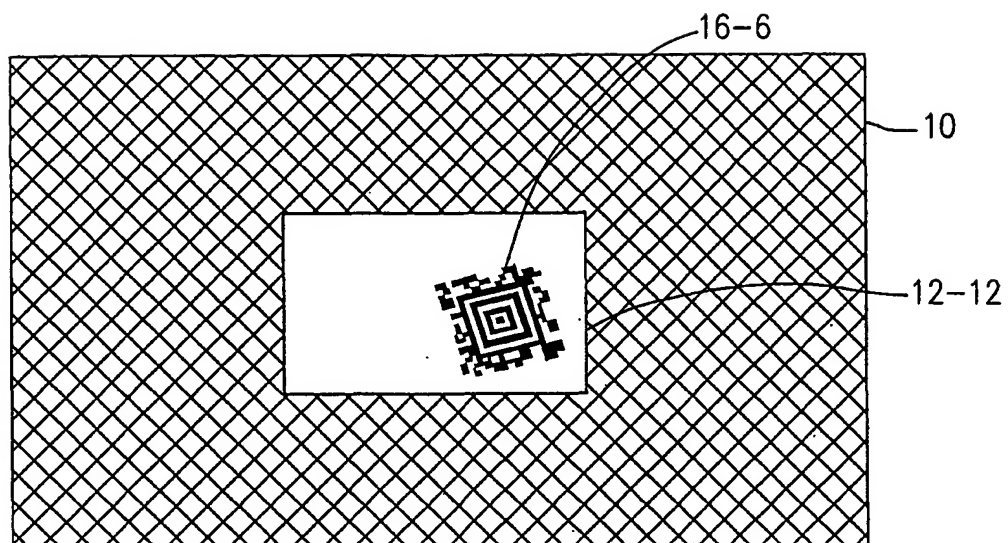


FIG. 1f

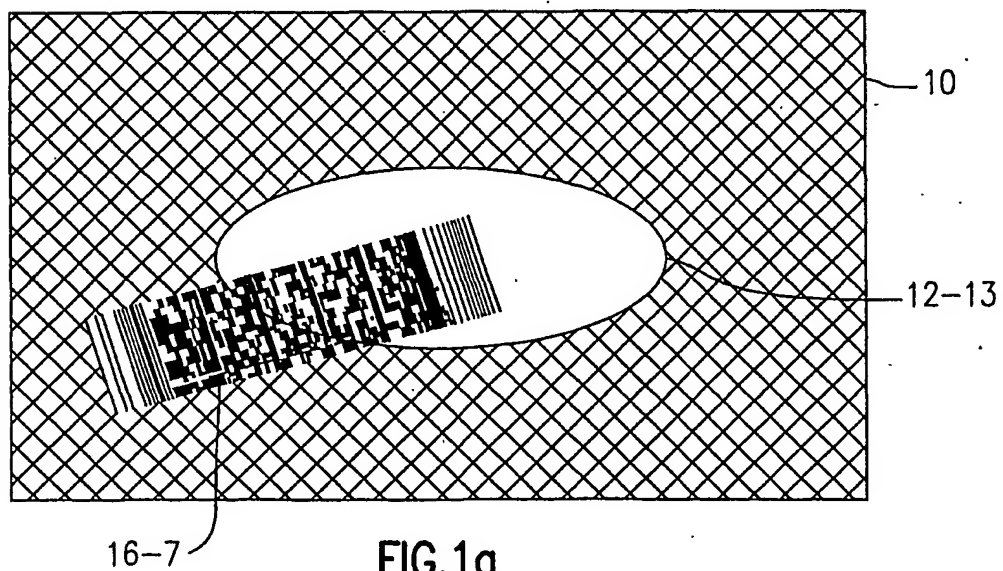


FIG. 1g

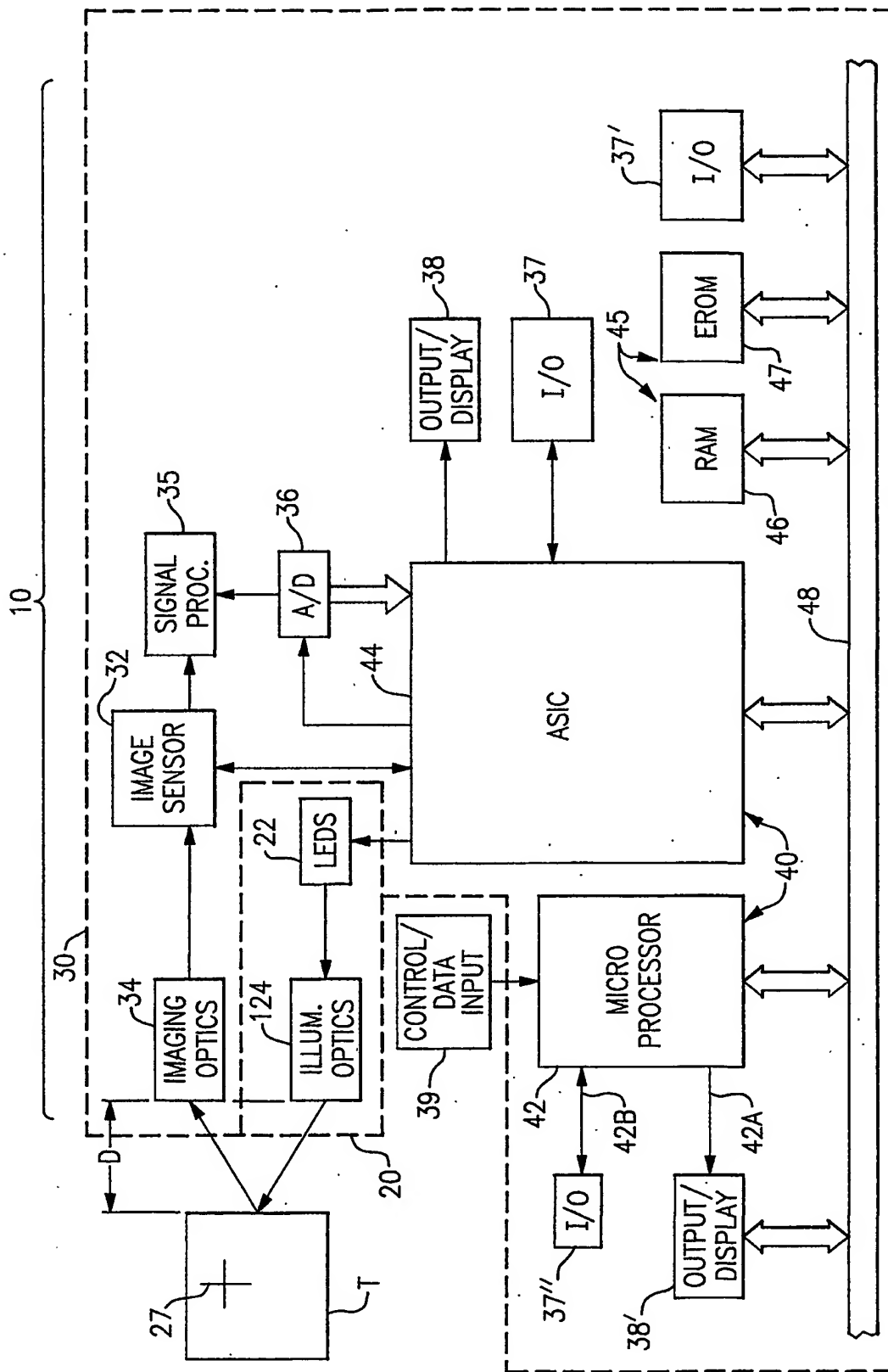
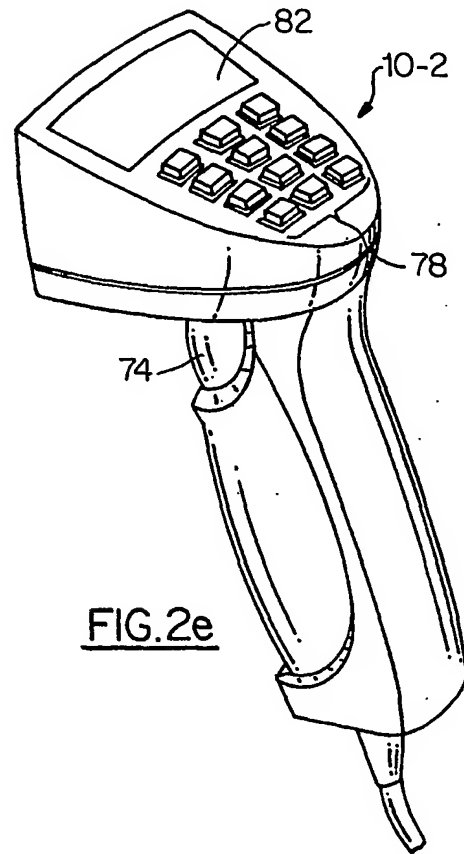
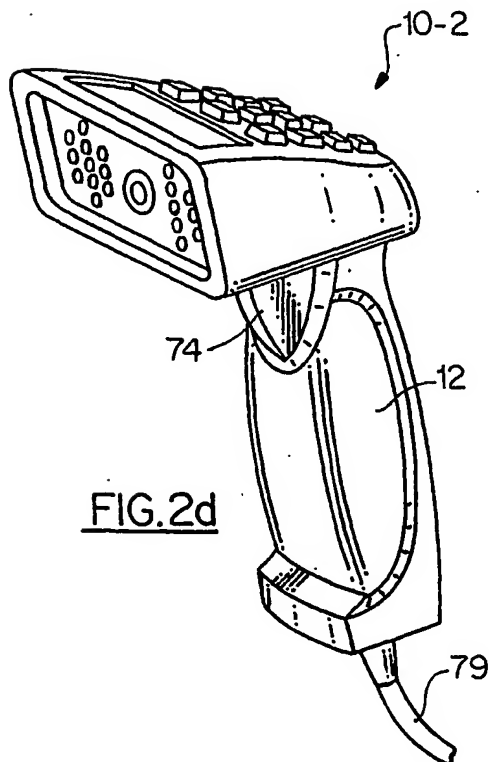
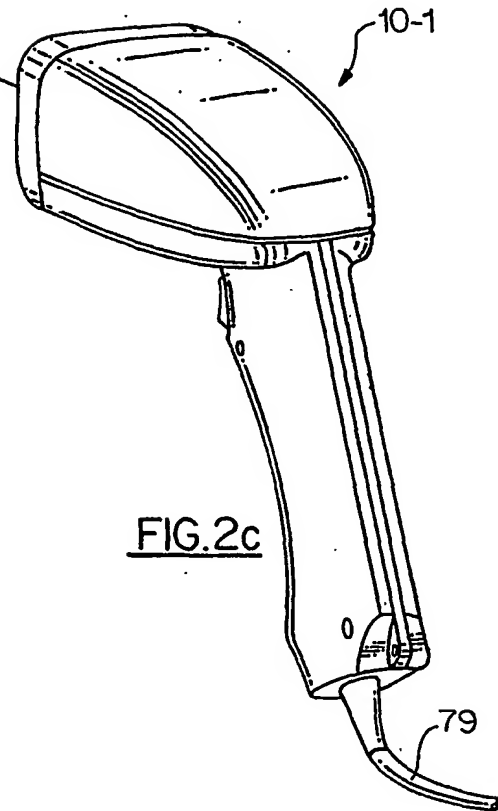
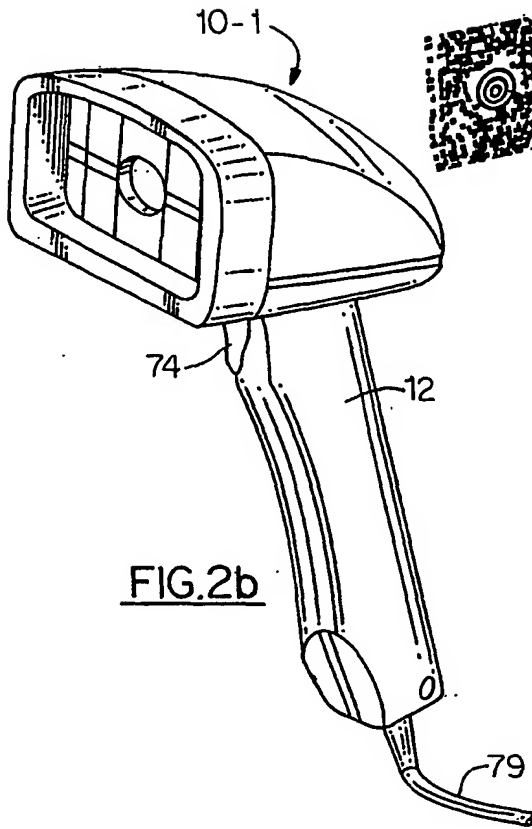
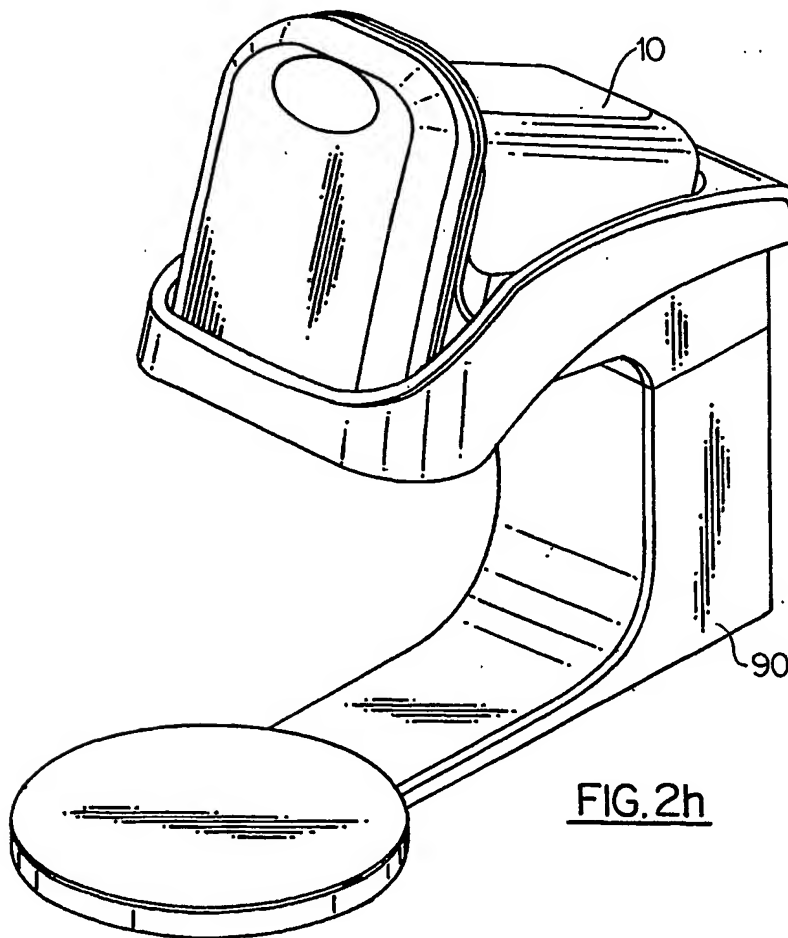
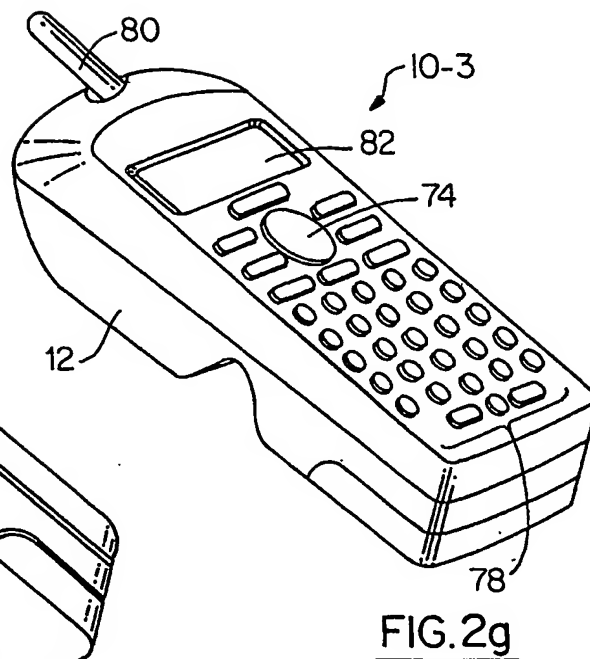
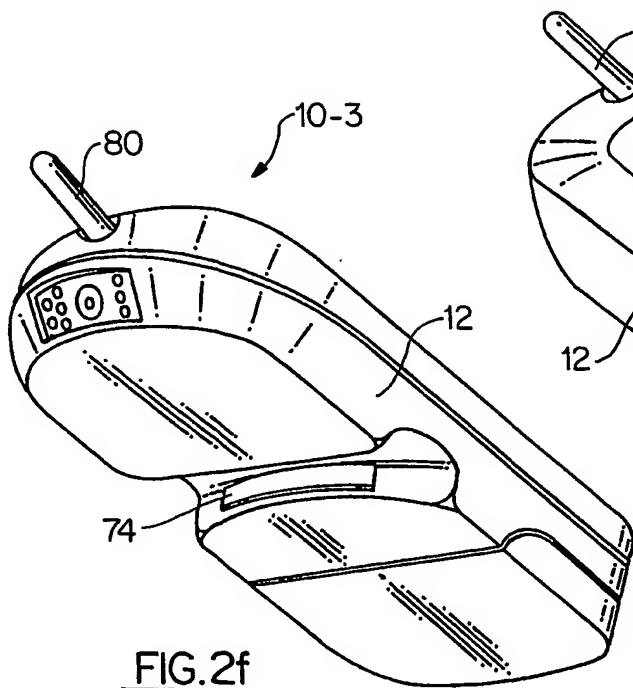
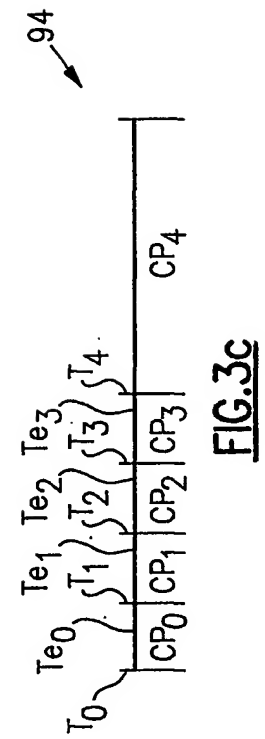
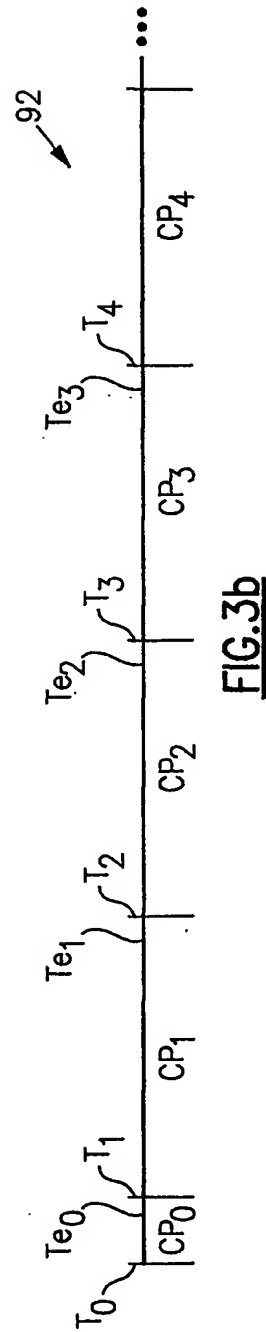
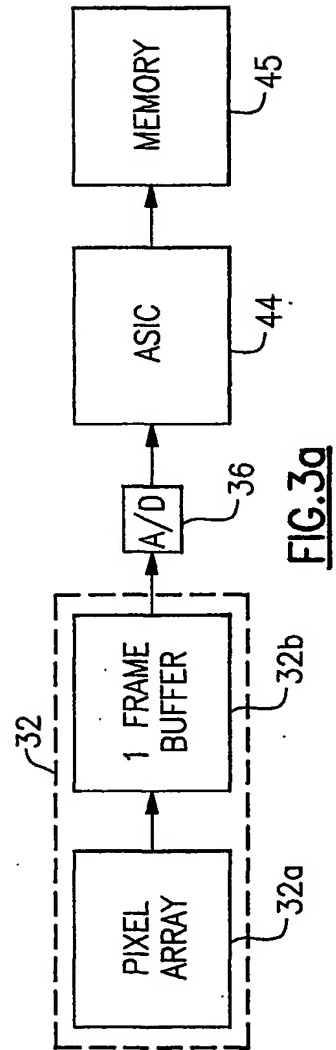
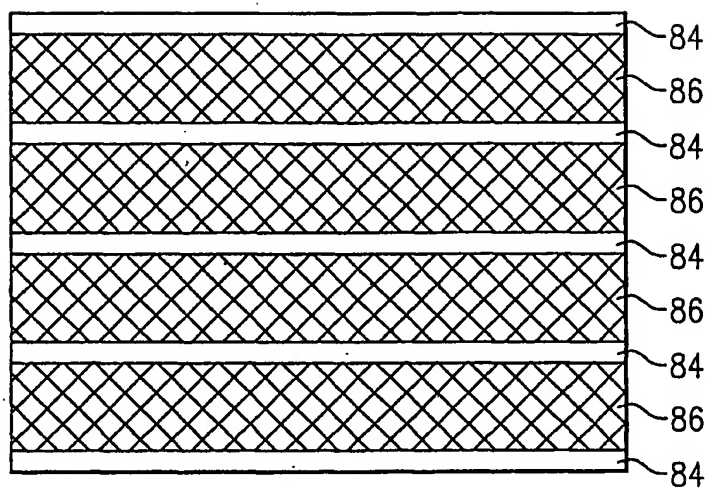
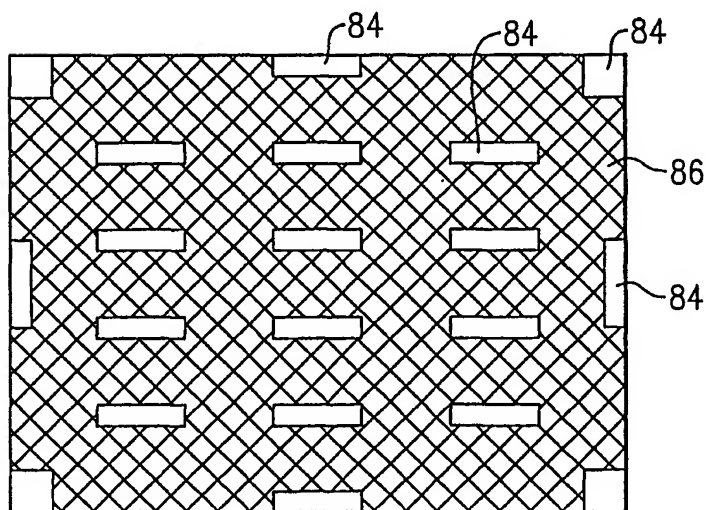


FIG. 2a







FIG.4aFIG.4b